HITIK KUMAR NAYAK

Junior Research Fellow (JRF) — VLSI & ASIC Design — Electronics & Communication Engineer

Balasore, Odisha, India

7978594517 hitikkumarnayak22@gmail.com Portfolio

TECHNICAL SKILLS

EDA & VLSI Tools: Cadence Virtuoso Suite (Schematic Capture, Layout XL), Mentor Graphics Calibre (nmDRC, LVS, PEX), LTspice, OriginPro, XCircuit

Analog IC Design: Two-Stage CMOS Op-Amp Architecture, Transistor Sizing (W/L), Differential Amplifiers, Bias Circuitry, Miller Frequency Compensation, Loop Stability Analysis, Noise, Common-Mode Rejection Ratio (CMRR) Optimization

Physical Verification & Tape-Out: Symmetrical Layout Placement, Device Matching (Common-Centroid, Cross-Coupling), Guard Rings, Dummy Layout Insertion, Parasitic-Aware Layout Routing, IO Pad Ring Integration, Automated Fill Generation, SCL 180nm ASIC Flow

Programming & Frameworks: Python, MATLAB, HTML, CSS, JavaScript, LaTeX (Advanced Technical Writing), Git/GitHub Version Control

PROFESSIONAL EXPERIENCE

Junior Research Fellow (JRF) Dec 2025 – Present
ABV-IIITM Gwalior Gwalior, India
MeitY Sponsored C2S Project – Implantable Pacemaker Chip (iPACE-CHIP)

- Developed **ultra-low-power analog/mixed-signal circuit blocks** for an **implantable pacemaker chip** using **Cadence**, performing **schematic design**, **custom layout**, **DRC/LVS verification**, and **physical design validation** for **MPW tape-out**.

Graduate Engineer Trainee (Electrical) Jun 2025 – Jul 2025
MSP Steel & Power Ltd. Raigarh, India

- Monitored **industrial substations**, **power distribution systems**, and **automated electrical controls** while performing **system diagnostics** and preparing **preventive maintenance documentation** for **high-voltage electrical infrastructure**.

PROJECTS

Custom Two-Stage CMOS Op-Amp ASIC Design & Tape-Out **[GitHub Link]**

- Designed a differential op-amp with schematic testbenches for **CMRR/ICMR**, developed custom **common-centroid Layouts** with dummy structures, and achieved **Calibre nmDRC/LVS sign-off** and **PEX** post-layout simulations to integrate the block into a **I/O Pad Ring** with seal rings for a complete **GDSII** tape-out flow using **SCL 180nm Flow**.

Summer Research Internship: 20T Hybrid Full Adder **[GitHub Link]**

- Designed and simulated a low-power **20T Hybrid Full Adder** in **LTspice** using conventional CMOS and **FinFET** technologies, analyzing short-channel effects, leakage current, and power-delay product (PDP) optimization.

Major Project: Channel Capacity Optimization of 6G System **[GitHub Link]**

- Scripted analytical channel simulators in **MATLAB** to evaluate communication behavior across **sub-THz allocations (50–200 GHz)**. Modeled localized atmospheric constraints, and molecular absorption variables to maximize **spectral efficiency metrics** against varying system operational distances.

INTERNSHIP EXPERIENCE

Intern – Electronics & Communication Engineering Department May 2024 – Jun 2024
National Institute of Technology (NIT) Raipur Raipur, India
Supervisor: Dr. Chitrakant Sahu (Associate Professor)

- Modeled and validated performance profiles for **Hybrid Full Adders** and standard sub-micron **CMOS inverter topologies** using **LTspice**.
- Simulated multi-gate **3D FinFET structures** to study sub-threshold logic swing, absolute **Power-Delay Product (PDP)**, and **Fan-out-of-4 (FO-4)** performance degradation boundaries across physical scale translations.

EDUCATION

Bachelor of Technology (B.Tech) – Electronics & Communication Engineering 2021 – 2025
Guru Ghasidas Vishwavidyalaya (GGU), Bilaspur, Chhattisgarh **CGPA: 7.62 / 10.0**

CERTIFICATIONS & ACHIEVEMENTS

- **GATE 2026 Qualified:** Electronics & Communication Engineering (ECE) — **Score: 434**
- **TCS NQT Cognitive Qualification:** Dec 2025 — National Percentile Score: **73.66%**
- **LaTeX for Advanced Technical Writing Certification:** Issued Feb 2025
- **National Level Participant:** SUSTAIN-A-THON 2024 organized by Indian Oil Corporation Limited (IOCL)